What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate having a surface;

a gate electrode formed over the surface of said semiconductor substrate with a gate dielectric film interposed therebetween;

a pair of source and drain diffusion layers formed in said semiconductor substrate to oppose each other with a channel region laterally residing therebetween at a location immediately beneath said gate electrode, said source and drain diffusion layers each having a low resistivity region and an extension region being formed to extend from this low resistivity region toward said channel region and being lower in impurity concentration and shallower in depth than said low resistivity region;

a first impurity doped layer of a first conductivity type formed in said channel region between the source/drain diffusion layers;

a second impurity doped layer of a second conductivity type formed under said first impurity doped layer; and

a third impurity doped layer of the first conductivity type formed under said second impurity doped layer, wherein

said first impurity doped layer is equal to or less in junction depth than the extension region of each of said source/drain diffusion layers, and wherein

said second impurity doped layer is determined in impurity concentration and thickness to ensure that this

layer is fully depleted due to a built-in potential creatable between said first and third impurity doped layers.

2. The device according to claim 1, wherein

said first impurity doped layer is set in impurity concentration and thickness to be fully depleted upon formation of a channel inversion layer.

3. The device according to claim 1, wherein

said first impurity doped layer is set in impurity concentration and thickness to be partially depleted upon formation of a channel inversion layer.

4. The device according to claim 1, wherein

each of said first and second impurity doped layers is formed by ion implantation of an impurity into an undoped semiconductor layer as has been epitaxially grown on said semiconductor substrate with said third impurity doped layer formed therein.

5. The device according to claim 1, wherein

said second impurity doped layer is selectively formed in a region immediately beneath said gate electrode.

6. The device according to claim 4, wherein

said second impurity doped layer is selectively formed in a region of said undoped semiconductor layer just beneath said gate electrode, and wherein

said source/drain diffusion layers are formed so that a bottom surface of the low resistivity region resides within said undoped semiconductor layer whereas a bottom surface of the extension region is in contact with said second impurity

doped layer.

7. The device according to claim 1, further comprising:

fourth impurity doped layers of the first conductivity type as embedded to be in contact with the extension regions of said source and drain diffusion layers.

8. The device according to claim 1, wherein the low resistivity regions of said source/drain diffusion layers are formed to have top surfaces higher in level than said gate dielectric film.

9. The device according to claim 1, wherein

said gate electrode has a metal film as contacted with the gate dielectric film.

10. The device according to claim 2, wherein

said gate electrode is formed of a metal film.

11. The device according to claim 3, wherein

said gate electrode is formed of a poly-silicon film.

12. A semiconductor device comprising:

a semiconductor substrate having a surface;

a gate electrode as formed over the surface of said semiconductor substrate with a gate dielectric film sandwiched therebetween;

a pair of source and drain diffusion layers formed in said semiconductor substrate to oppose each other with a channel region laterally interposed therebetween at a location immediately beneath said gate electrode;

a first impurity doped layer of a first conductivity

type formed in said channel region between the source/drain diffusion layers;

a second impurity doped layer of a second conductivity type formed under said first impurity doped layer; and

a third impurity doped layer of the first conductivity type formed under said second impurity doped layer, wherein

said first impurity doped layer is equal to or less in junction depth than said source/drain diffusion layers, and wherein

said second impurity doped layer is determined in impurity concentration and thickness causing a depth of its junction with said third impurity doped layer to be greater than a junction depth of said source/drain diffusion layers while permitting said second impurity doped layer to be fully depleted due to a built-in potential creatable between said first and third impurity doped layers.

13. The device according to claim 12, wherein

said source/drain diffusion layers each comprise a low resistivity region and an extension region being formed to extend from this low resistivity region toward said channel region and being lower in impurity concentration and shallower in depth than said low resistivity region, said low resistivity region having a bottom surface residing within said second impurity doped layer.

14. The device according to claim 12, wherein

said first impurity doped layer is determined in impurity concentration and thickness to be fully depleted

upon formation of a channel inversion layer.

15. The device according to claim 12, wherein

said first impurity doped layer is determined in impurity concentration and thickness to be partially depleted upon formation of a channel inversion layer.

16. The device according to claim 12, wherein

Each of said first and second impurity doped layers is formed through ion implantation of an impurity into an undoped semiconductor layer as has been epitaxially grown on said semiconductor substrate with said third impurity doped layer formed therein.

17. The device according to claim 12, wherein

said second impurity doped layer is selectively formed in a region right beneath said gate electrode.

18. The device according to claim 16, wherein

said second impurity doped layer is selectively formed in a region of said undoped semiconductor layer just beneath said gate electrode, and wherein

said source/drain diffusion layers each comprise a low resistivity region having its bottom surface residing within said undoped semiconductor layer and an extension region formed to extend from this low resistivity region toward said channel region to have a bottom surface in contact with said second impurity doped layer, the extension region being lower in impurity concentration and shallower in depth than said low resistivity region.

19. The device according to claim 13, further

comprising:

fourth impurity doped layers of the first conductivity type as embedded to be in contact with the extension regions of said source/drain diffusion layers.

20. The device according to claim 13, wherein

the low resistivity regions of said source/drain diffusion layers are formed to have top surfaces higher in level than said gate dielectric film.

21. The device according to claim 12, wherein

said gate electrode has a metal film as contacted with the gate dielectric film.

22. The device according to claim 14, wherein

said gate electrode is formed of a metal film.

23. The device according to claim 15, wherein

said gate electrode is formed of a poly-silicon film.

24. A semiconductor device comprising:

a semiconductor substrate having a surface;

a gate electrode formed over the surface of said semiconductor substrate with a gate dielectric film sandwiched therebetween;

source and drain diffusion layers formed in said semiconductor substrate to oppose each other with a channel region laterally residing therebetween at a location immediately beneath said gate electrode, said source and drain diffusion layers each having a low resistivity region and an extension region being formed to extend from this low resistivity region toward said channel region and being

lower in impurity concentration and shallower in depth than said low-resistivity region;

a first impurity doped layer of a first conductivity type formed in said channel region between the source/drain diffusion layers;

a second impurity doped layer of a second conductivity type formed under said first impurity doped layer; and

a third impurity doped layer of the first conductivity type formed under said second impurity doped layer, wherein

said first impurity doped layer is selectively formed in such a manner as to be greater in junction depth than the extension regions of said source/drain diffusion layers while being determined in impurity concentration and thickness to be partially depleted upon formation of a channel inversion layer, and wherein

said second impurity doped layer is selectively formed to have its opposite end portions in contact with the extension regions of said source and drain diffusion layers while having an impurity concentration and a thickness as determined to ensure that said second impurity doped layer is fully depleted due to a built-in potential creatable between the first and third impurity doped layers.

25. The device according to claim 24, wherein

said first impurity doped layer is surrounded by a depletion layer being formed between it and the extension regions of said source/drain diffusion layers and said second impurity doped layer that is fully depleted to

thereby be set in a floating state.

26. A semiconductor device comprising:

a semiconductor substrate;

a first transistor having first source and drain diffusion layers formed in said semiconductor substrate and a first gate electrode formed between the first source/drain diffusion layers of said semiconductor substrate with a gate dielectric film sandwiched between said substrate and said first gate electrode; and

a second transistor having second source and drain diffusion layers formed in said semiconductor substrate and a second gate electrode formed between the second source/drain diffusion layers of said semiconductor substrate with a gate dielectric film sandwiched between said substrate and said second gate electrode, wherein

said first transistor further comprises:

a first impurity doped layer of a first conductivity type formed in a channel region defined between said first source/drain diffusion layers;

a second impurity doped layer of a second conductivity type formed under said first impurity doped layer;

a third impurity doped layer of the first conductivity type formed under said second impurity doped layer;

said first impurity doped layer being equal to or less in junction depth than said first source/drain diffusion layers and being determined in impurity concentration and thickness to be fully or partially depleted upon formation

of a channel inversion layer; and

said second impurity doped layer having a depth of junction with said third impurity doped layer greater than that of said first source/drain diffusion layers while being determined in impurity concentration and thickness to be fully depleted due to a built-in potential creatable between the first and third impurity doped layers.

27. The device according to claim 26, wherein

said second transistor has at a portion of said semiconductor substrate just beneath said second gate electrode a bulk layer of the first conductivity type formed as an impurity doped layer deeper than said second source/drain diffusion layers.

28. The device according to claim 26, wherein

said second transistor further comprises:

a fourth impurity doped layer of the first conductivity type formed in a channel region between said second source/drain diffusion layers;

a fifth impurity doped layer of the second conductivity type formed under said fourth impurity doped layer;

a sixth impurity doped layer of the first conductivity type formed under said fifth impurity doped layer;

said fourth impurity doped layer being equal to or less in junction depth than said first impurity doped layer of said first transistor and is determined in impurity concentration and thickness to be partially depleted upon formation of a channel inversion layer; and

said fifth impurity doped layer having a depth of junction with said sixth impurity doped layer greater than that of said second source/drain diffusion layers while being set in impurity concentration and thickness to be fully depleted due to a built-in potential creatable between the fourth and sixth impurity doped layers.

29. A NAND gate circuit formed in a semiconductor substrate, comprising a plurality of n-channel transistors serially connected between a ground terminal and an output terminal with the respective gates serving as input terminals, and a plurality of p-channel transistors connected in parallel with each other between a power supply terminal and the output terminal with the respective gates connected to the input terminals, wherein

said n-channel transistors each comprises:

a first gate electrode as formed over a surface of said semiconductor substrate with a gate dielectric film sandwiched therebetween;

first source/drain diffusion layers formed in said semiconductor substrate to oppose each other with a channel region laterally interposed therebetween at a location immediately beneath said gate electrode;

a first p-type impurity doped layer formed in the channel region between said first source/drain diffusion layers;

an n-type impurity doped layer formed under said first p-type impurity doped layer;

a second p-type impurity doped layer formed under said n-type impurity doped layer;

said first p-type impurity doped layer being equal to or less in junction depth than said first source/drain diffusion layers; and

said n-type impurity doped layer being determined in impurity concentration and thickness causing a depth of its junction with said second p-type impurity doped layer to be greater than a junction depth of said first source/drain diffusion layers while permitting said n-type impurity doped layer to be fully depleted due to a built-in potential creatable between said first and second p-type impurity doped layers, and wherein

said p-channel transistors each comprises:

a second gate electrode as formed over the surface of said semiconductor substrate with a gate dielectric film sandwiched therebetween;

second source/drain diffusion layers formed in said semiconductor substrate to oppose each other with a channel region laterally interposed therebetween at a location immediately beneath said second gate electrode; and

a bulk layer formed in the channel region between said second source/drain diffusion layers to be deeper than said second source/drain diffusion layers.

30. A dynamic circuit formed in a semiconductor substrate, comprising a plurality of switching transistor disposed between first and second nodes in parallel with

each other of which gates serve as input terminals, a precharging transistor of which gate is driven by a control signal for precharging the first node to a predetermined potential, and an activating transistor of which gate is driven by a clock signal for connecting the second node to a ground terminal, wherein

said switching transistors each comprises:

a first gate electrode as formed over a surface of said semiconductor substrate with a gate dielectric film sandwiched therebetween;

first source/drain diffusion layers formed in said semiconductor substrate to oppose each other with a channel region laterally interposed therebetween at a location immediately beneath said first gate electrode;

a first impurity doped layer of a first conductivity type formed in the channel region between said first source/drain diffusion layers;

a second impurity doped layer of a second conductivity type formed under said first impurity doped layer; and

a third impurity doped layer of the first conductivity type formed under said second impurity doped layer;

said first impurity doped layer being equal to or less in junction depth than said source/drain diffusion layers; and

said second impurity doped layer being determined in impurity concentration and thickness causing a depth of its junction with said third impurity doped layer to be greater

than a junction depth of said first source/drain diffusion layers while permitting said second impurity doped layer to be fully depleted due to a built-in potential creatable between said first and third impurity doped layers, and wherein

said prechaging transistor and activating transistor each comprises:

a second gate electrode as formed over the surface of said semiconductor substrate with a gate dielectric film sandwiched therebetween;

second source/drain diffusion layers formed in said semiconductor substrate to oppose each other with a channel region laterally interposed therebetween at a location immediately beneath said second gate electrode; and

a bulk layer formed in the channel region between said second source/drain diffusion layers to be deeper than said second source/drain diffusion layers.

31. A NAND gate circuit formed in a semiconductor substrate, comprising a plurality of n-channel transistors serially connected between a ground terminal and an output terminal with the respective gates serving as input terminals, and a plurality of p-channel transistors connected in parallel with each other between a power supply terminal and the output terminal with the respective gates connected to the input terminals, wherein

said semiconductor substrate has an SOI structure region in which an insulating film is buried in a

predetermined position in depth and a bulk region, and wherein

said n-channel transistors are formed as SOIFETs in said SOI structure region, and wherein

said p-channel transistors are formed as bulk FETs in said bulk region.

32. A dynamic circuit formed in a semiconductor substrate, comprising a plurality of switching transistors disposed between first and second nodes in parallel with each other of which gates serve as input terminals, a precharging transistor of which gate is driven by a control signal for precharging the first node to a predetermined potential, and an activating transistor of which gate is driven by a clock signal for connecting the second node to a ground terminal, wherein

said semiconductor substrate has an SOI structure region in which an insulating film is buried in a predetermined position in depth and a bulk region, and wherein

said switching transistors are formed as SOIFETs in said SOI structure region, and wherein

said precharging transistor and activating transistor are formed as bulk FETs in said bulk region.

33. A method of fabricating a semiconductor device comprising:

letting a first semiconductor layer with no impurity doped therein epitaxially grow on a semiconductor substrate

having in at least its surface a first impurity doped layer of a first conductivity type;

performing ion implantation into said first semiconductor layer to form a second impurity doped layer of a second conductivity type as contacted with said first impurity doped layer;

forming through ion implantation into a surface portion of said first semiconductor layer a third impurity doped layer of the first conductivity type in contact with said second impurity doped layer;

forming above said third impurity doped layer a gate electrode with a gate dielectric film sandwiched therebetween; and

forming in said semiconductor substrate source and drain diffusion layers being self-aligned with said gate electrode and each having a junction depth deeper than a junction between said third impurity doped layer and said second impurity doped layer and yet shallower than a junction between said second impurity doped layer and said first impurity doped layer.

34. The method according to claim 33, wherein

said forming of the source and drain diffusion layers comprises:

performing ion implantation into said third impurity doped layer with said gate electrode being as a mask therefor to form fourth impurity doped layers for use as source and drain extension regions;

forming a sidewall dielectric film on a lateral wall of said gate electrode;

selectively epitaxially growing a second semiconductor layer on said fourth impurity doped layers; and

performing ion implantation into said second semiconductor layer with both said gate electrode and said sidewall dielectric film as a mask to form fifth impurity doped layers for use as source and drain low-resistivity regions greater in depth and higher in impurity concentration than said fourth impurity doped layers.

35. The method according to claim 33, further comprising:

forming, prior to the epitaxially growing of said first semiconductor layer, an element isolation dielectric film at said semiconductor substrate.

36. The method according to claim 33, further comprising:

forming, after having formed said third impurity doped layer, an element isolation dielectric film at said semiconductor substrate.

37. The method according to claim 33, wherein

said second impurity doped layer is formed to have such an impurity concentration and a thickness as to be fully depleted due to a built-in potential between the first and third impurity doped layers.

38. The method according to claim 33, wherein

said third impurity doped layer is formed to have such

an impurity concentration and a thickness as to be fully depleted upon formation of a channel inversion layer.

39. The method according to claim 33, wherein said third impurity doped layer is formed to have such an impurity concentration and a thickness as to be partially depleted upon formation of a channel inversion layer.

40. A method of fabricating a semiconductor device comprising:

letting a first impurity non-doped semiconductor layer epitaxially grow on a semiconductor substrate having in at least its surface a first impurity doped layer of a first conductivity type;

performing ion implantation into the first semiconductor layer to form a second impurity doped layer of a second conductivity type as contacted with said first impurity doped layer;

letting a second impurity non-doped semiconductor layer epitaxially grow on said second impurity doped layer;

doing ion implantation into the second semiconductor layer to form a third impurity doped layer of the first conductivity type as contacted with said second impurity doped layer;

forming above said third impurity doped layer a gate electrode with a gate dielectric film being sandwiched therebetween; and

forming in said semiconductor substrate source and drain diffusion layers being self-aligned with said gate

electrode and each having a junction depth deeper than a junction between said third impurity doped layer and said second impurity doped layer and yet shallower than a junction between said second impurity doped layer and said first impurity doped layer.

41. The method according to claim 40, wherein

said forming of the source and drain diffusion layers comprises:

performing ion implantation into said third impurity doped layer with said gate electrode being as a mask to form fourth impurity doped layers deeper than said third impurity doped layer for use as source and drain extension regions;

forming a sidewall dielectric film on a lateral wall of said gate electrode;

selectively epitaxially growing a third semiconductor layer on said fourth impurity doped layers; and

doing ion implantation into said third semiconductor layer with both said gate electrode and said sidewall dielectric film as a mask to form fifth impurity doped layers for use as source and drain low resistivity regions greater in depth and higher in impurity concentration than said fourth impurity doped layers.

42. The method according to claim 40, further comprising:

forming, prior to the epitaxially growing of said first semiconductor layer, an element isolation dielectric film at said semiconductor substrate.

43. The method according to claim 40, further comprising:

forming, after having formed said third impurity doped layer, an element isolation dielectric film at said semiconductor substrate.

44. The method according to claim 40, wherein

said second impurity doped layer is formed to have such an impurity concentration and a thickness as to be fully depleted due to a built-in potential between the first and third impurity doped layers.

45. The method according to claim 40, wherein

said third impurity doped layer is formed to have such an impurity concentration and a thickness as to be fully depleted upon formation of a channel inversion layer.

46. The method according to claim 40, wherein

said third impurity doped layer is formed to have such an impurity concentration and a thickness as to be partially depleted upon formation of a channel inversion layer.